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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,537	02/12/2002	Shahla Khorram	BP 2133	7244

7590 08/11/2005

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EXAMINER	
NGUYEN, DUC M	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,537	KHORRAM, SHAHLA	
	Examiner	Art Unit	
	Duc M. Nguyen	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC ∋ 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-5, 16-18** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Hayashi** (US **6,366,172**) in view of **Yamaguchi** (US Patent Number **6,804,500**).

Regarding claims **1, Hayashi** discloses a highly linear power amplifier comprises :

- a component (see Z_L in Figs. 1, 4);
- first transistor pair coupled in series with the component, wherein a first transistor (101) of the first transistor pair is coupled to receive an input signal and wherein a second transistor (102) of the first transistor pair is coupled to receive a first enable signal (V_b);

However, Hayashi fails to disclose a second transistor pair coupled in parallel with the first transistor pair. However, Yamaguchi discloses an amplifier wherein the amplifier is formed by three amplifier blocks coupled in parallel, each block having a difference enable signal Vcnt and a difference output gain (see Fig. 12 and col. 10, line 28 – col. 11, line 22), for improving wide dynamic range of the amplifier. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the above teachings of Hayashi and Yamaguchi for implement each amplifier

block in Yamaguchi with a transistor pair in Hayashi, thereby result in a second transistor pair in parallel with the first transistor pair as claimed, for providing a wide dynamic range power amplifier.

Regarding claim **16**, the claim is rejected for the same reason as set forth in claim 1 above, wherein it would have been obvious to one skilled in the art at the time the invention was made to replace the singe-ended amplifier (Fig. 1 of Hayashi) with the differential amplifier (Fig. 2 of Hayashi) as well and would work equally well, for utilizing advantages of differential signals such as low noise figure (i.e, noises tends to cancel out when combining differential signals).

Regarding claim **2**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, **Hayashi** discloses the component comprise at least one resistor or inductor as claimed (see Fig. 15).

Regarding claim **3**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, since Yamaguchi also discloses a third amplifier block, it is clear that Hayashi and Yamaguchi as modified would disclose at least one other transistor pair as claimed, for further widening dynamic range of the amplifier.

Regarding claim **4**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, since **Yamaguchi** discloses high, medium and low output amplifier cell block (see col. 10, lines 28-37) and that a gain of a transistor is proportional to its size (see col. 17, lines 20-23), it is clear that Hayashi and Yamaguchi as modified would disclose the first gain is greater than the second gain, and the first size is greater than the second size with a ratio as claimed.

Regarding claim **5**, the claim is interpreted and rejected for the same reason as set forth in claim 16 above, wherein it is clear that the differential transistor pair would comprise a first complimentary and second complimentary transistor pair as claimed.

Regarding claims **17-18**, the claims are interpreted and rejected for the same reason as set forth in claim **5** above, wherein it is clear that the differential transistor pair would comprise p-channel or n-channel transistor as claimed (see Hayashi, col. 9, lines 58-60).

3. Claims **6-15** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Hayashi** in view of **Yamaguchi** and further in view of **Hans** (US Patent Number **5,923,215**).

Regarding claim **6**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, Yamaguchi discloses a control module to generate the first and second control (or enable) signals (see col. 12, lines 51-59). However, Yamaguchi fails to disclose the control signal is based on desired output levels of the amplifier. However, such control signal based on desired output levels of the amplifier is well known in the art as disclosed by Hans (see Fig. 1). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching of Hans to Hayashi and Yamaguchi for providing control signals based on desired output levels of the amplifier as claimed, for controlling output power in order to minimize interferences, or reduce power consumption.

Regarding claim **7**, the claim is interpreted and rejected for the same reason as set

forth in claims 4 and 6 above, wherein it it is clear that the cumulative gain is a combination of two gains and thus would greater than either the first gain or the second gain.

Regarding claim **8**, the claim is rejected for the same reason as set forth in claims 1, 6 above. In addition, Yamaguchi discloses an upconverter (see Fig. 20A, ref. 106 regarding the modulator) and that it would have been obvious to one skilled in the art to utilize I-Q components (also known as differential signals) for IF signal as claimed, for utilizing advantages of differential signals such as low noise figure (i.e, noises tends to cancel out when combining differential signals).

Regarding claims **9-15**, the claims are interpreted and rejected for the same reason as set forth in claim **8** above. Inaddition, since Yamaguchi also discloses a third amplifier block, it is clear that Hayashi and Yamaguchi as modified would disclose at least one other transistor pair as claimed, for further widening dynamic range of the amplifier. Further, it would have been obvious to one skilled in the art at the time the invention was made to replace the singe-ended amplifier (Fig. 1 of Hayashi) with the differential amplifier (Fig. 2 of Hayashi) as well and would work equally well, for utilizing advantages of differential signals such as low noise figure (i.e, noises tends to cancel out when combining differential signals).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Weber (US 6,504,433), CMOS transceiver having an integrated power amplifier.

Jett, Jr. et al (US 4,520,324), MOS gain controlled amplifier.

Barak et al (US 6,587,511), Radio frequency transmitter and method thereof.

Sevic et al (US 6,137,355), Dual-mode amplifier with high efficiency and high linearity.

5. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for formal communications intended for entry)

(571)-273-7893 (for informal or draft communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Or to Edward Urban (Supervisor) whose telephone number is (571) 272-7899.

Duc M. Nguyen

July 28, 2005